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(54) Closed loop and open loop synchronization of the phase switchings in driving a DC motor

Synchronisation der geregelten und der gesteuerten Phasenansteuerung von Gleichstrommotoren

Synchronisation du pilotage en boucle fermée et en boucle ouverte des interrupteurs de phase d'un moteur à courant continu

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Description

[0001] The present invention relates in general to techniques for driving an electronically switched electric motor. In particular the invention relates to a synchronizing circuit of the phase switchings in a open loop or closed loop functioning mode, using predefined signals digitally stored in a nonvolatile read only memory.

[0002] Recently, a new driving technique has been developed for motors electronically switched according to a preestablished profile, typically sinusoidal, digitized and stored in a ROM memory in the form of an N number of samples.

[0003] A driving current or voltage coherent with such a predefined profile is forced into each respective phase windings of a motor in synchronism with the rotor position, which may be detected by way of dedicated sensors or, as generally done, by sensing the zero cross instant of back-electromotive-forces induced on the phase windings of the motor.

[0004] Usually, this synchronizing function is carried out by measuring the interval of time (period) between two successive zero crossings of the back-electromotive-forces signal or signals, and by using a frequency multiplier (e.g. a clock signal divider) to drive the pointer of the digital sample of the predefined and stored profile, represented by the N digital samples stored in the ROM memory, synchronizing the phase switchings with this instantaneous value of the period between two successive zero crossings.

[0005] An entirely digital driving system of this kind is described in the prior European patent application EP 0809349, while dedicated reconstruction systems of back-electromotive-forces signals to synchronize the driving of sensorless motors are described in the prior European patent applications EP 0822649 and EP 0782268, by the same applicant.

[0006] These entirely digital driving systems, may be alternatively commanded to operate in a closed loop mode or in an open loop mode of the synchronization control, during which the switching frequency may be imposed by writing in a dedicated register a certain frequency datum for driving the phase switching to correspond to N times the desired rotation speed.

[0007] When the system is commanded to function again in a closed loop mode, for example during accelerations or decelerations from a steady state speed, a command is sent to ensure that the synchronizing system uses for the successive phase switching the time period between a forced synchronization signal, that is of a pseudo zero crossing, and the pulse of the first real zero crossing, the successive scanning periods will obviously use the time interval lapsing between two successive real zero crossings, according to a normal closed loop mode of synchronization.

[0008] The ability to switch from an open loop and a closed loop mode of operation is implemented in the known systems by way of a relatively complex circuitry. In the prior art document US 5223772 for example, the synchronisation of the output of an internally-driven VCO to an exterior clock signal is obtained by using the exterior clock signal to restart the VCO at every exterior clock pulse, until the preset VCO frequency is reached. At that point, the restarting of the VCO ceases, and the VCO locks onto the internal signal it is designed to track. Moreover in systems functioning in a voltage mode it is necessary to employ special means for introducing a certain phase shift for compensating for the phase angle existing between the drive current flowing in the windings and the voltage applied thereto.

[0009] It has now been found and constitutes the object of the present invention a synchronizing circuit particularly simple and switchable from a closed loop made to an open loop functioning mode and viceversa, in a perfectly reliable manner, by simply adding a minimum number of elements to a normal closed loop synchronizing circuit.

[0010] Moreover, the circuit of the invention may, by adding only one programmable register, introduce a certain phase shift between the predefined driving waveform profile and the back-electromotive-force waveform induced in the phase windings, that is in respect to the zero crossing instants of the back-electromotive-force in order to optimize torque characteristics and efficiency yield during a closed loop functioning phases of the synchronization system.

[0011] The circuit of the invention is defined in the annexed claim 1 while a preferred embodiment of the circuit of the invention is defined in the dependent claim.

[0012] The architecture, the functioning and the advantages of the circuit of the invention will be better illustrated by referring to an embodiment shown in the annexed drawings, wherein:

Figure 1 shows the diagram of a common closed loop synchronizing circuit, according to the prior art;

Figure 2 shows the diagram of a synchronizing circuit of the invention according to a preferred embodiment.

[0013] By referring to the figures, given a certain N number of samples representing the driving profile, the scanning frequency (fscan) of the profile defined by the sequence of the N digital samples stored in a ROM memory must be substantially synchronized in respect to the rotation speed of the motor in a manner that:

$$fscan = N * fc$$

wherein

$$fc = \frac{RPM}{60} * P$$

where P is the number of poles of the motor and RPM is the number of revolutions per minute.

[0014] In a digital driving system wherein there exists a system or master clock signal ck of a higher frequency than fscan, the circuit with which the necessary frequency multiplication to generate a pointer S, of a certain digital sample of the driving profile stored in a dedicated memory is effected, in synchronism with a signal of zero crossing ZCR, continuously sensed by dedicated sensors or extracted from reconstructed the back-electromotive-force induced in the stator windings by the rotor's rotation, is shown in Fig. 1.

[0015] The system clock signal ck drives the counter CONTSCAN and, through a divider by N, DIVN, it drives the counter CONTUP.

[0016] Upon the incoming of a (zero-cross) ZCR synchronizing pulse, the register REG A stores the datum contained in the counter CONTUP, which with the successive clock pulse ck resets itself and start again the counting until the successive ZCR.

[0017] The comparator compares the content of CONTSCAN, fed at the input B of the comparator, with the datum contained in the register REG A fed to the input A of the comparator and when these two data are equal, the comparator resets the counter CONTSCAN via a CLEAR command and generates a phase switching pulse fscan.

[0018] The fscan pulses increment the counter CONTN whose output datum S represents the value of the pointer to the ROM memory where the N samples are stored.

[0019] To generate a pulse of forced synchronization for operating in a open loop mode, and to thus provide for the possibility of switching between the open loop and closed loop functioning modes, as well as to allow optionally the programming of a certain phase shift of the driving (phase switchings) in respect to the real synchronizing pulses when functioning in a closed loop mode and in a voltage mode, the basic synchronizing circuit depicted in Fig. 1 is modified, according to the present invention, as shown in Fig. 2.

OPEN LOOP MODE OPERATION

[0020] When functioning in open loop mode, a certain value of the frequency of scan of the samples of the driving profile, predefined and permanently stored in the ROM memory, is programmable in the REG FT register. In these conditions of operation the signal CLOSE is at a certain logic value, for example "0", so as to reset the CONTUP counter which is used during closed loop operation. The demultiplexer from 1 to 2, (1*2) DEMUX, and the multiplexer from 2 to 1, (2*1) MUX, when the switching signal CLOSE=0, connect the output of the REG FT register to the input of the register REG A and therefore to the correspondent input A of the comparator.

[0021] Therefore in this mode of operation, the comparator compares the content of the programming register REG FT with the output of the counter CONTSCAN generating the fscan pulses.

[0022] The counter CONTN advances at each fscan pulse, counting from 0 to N-1.

[0023] Each time the counter N reaches N-1, it generates a signal WN which is fed to the circuit MSF FALSE.

[0024] The circuit MSF FALSE generates a forced synchronizing pulse ZCF that loads any new value programmed in the REG FT in the register REG A and so forth, so that, during open loop functioning, the profiles are scanned in synchronism with the forced ZCF synchronizing pulses.

SWITCHING FROM OPEN LOOP TO CLOSED LOOP MODE

[0025] The switching of the driving system from an open loop to a closed loop mode of the operation of synchronization control may be commanded by a logic command WAC sent to the circuit MSF FALSE.

[0026] At the instant the circuit MSF FALSE generates a new forced ZCF synchronizing pulse ZCF, if the logic command WAC is active, it sets the signal CLOSE to "1", thus removing the reset from the counter CONTUP, which starts to count measuring the interval of time between the forced ZCF synchronizing pulse and the next real ZCR synchronizing pulse.

[0027] The signal CLOSE=1 also couples, via the DEMUX demultiplexer, the output of the programming register REG FT to the input of the CONTSCAN counter and, through the multiplier MUX, the output of CONTUP to the input of the REG A register and sets ZCRF=ZCR.

CLOSED LOOP MODE OPERATION

[0028] Upon the incoming of a real synchronizing pulse ZCR, the content of the counter CONTUP is loaded in the register REG A, thus generating the fscan pulses between two successive ZCR pulses, similarly to what illustrated in relation to the basic scheme of figure 1

PROGRAMMING OF A CERTAIN PHASE SHIFT

[0029] The circuit of the invention lends itself also to the programming of a certain phase shift of the switchings of the winding of the motor in relation to the real synchronizing pulses ZCR. This becomes necessary or useful in the case of driving the windings of the motor in a voltage mode, for compensating for the phase difference between the driving voltage applied to their terminals and the current actually flowing through the windings (which generates the torque).

[0030] This function may be easily implemented by simply adding a second programmable register REG T A certain phase anticipation may be programmed by the use of the two registers REG T and REG FT.

[0031] A gross phase shift value is programmable in the REG T register, by which it is defined from which sample of the N samples that represent the preestablished profile stored in the ROM should start the counting of the counter CONTN, with which it forms a "cyclic counter", resettable to T (that is, counting from T to N-1 to T-1).

[0032] To this gross value of phase shift is added a dynamic phase shift value (fine) settable through the REG FT register, which determines the starting instant of the counter CONTSCAN within the phase interval of the Tth sample.

[0033] Upon the incoming of a new real synchronizing pulse (ZCR), the counter CONTN is reset to a programmed value contained in the programming register REG FT.

[0034] The circuit of the invention allows for the implementation of these important functions with a minimum number of components. The precision of the system may be easily fixed by the parameters N and the sizes of the counters and of the registers employed.

[0035] Advantageously, the same programming register REG FT may be used for different functions during both open loop operation functioning and closed loop operation; in the latter case, for establishing, in conjunction with the other programmable register REG T (specifically included added for this purpose), a programmable phase shift, with great precision.

Claims

1. A synchronizing circuit of the phase switchings of a multiphase brushless motor, according to a profile stored in a nonvolatile manner in the form of an N number of digital samples, selectively switchable in a open loop or closed loop mode of operation, comprising a frequency multiplier (DIVN) of a master clock signal (Ck) outputting a derived clock signal (Ck/N) whose period is divided by an N factor, a first resettable count-up counter (CONTUP) fed with said derived clock signal (Ck/N), a first register (REG A) storing the output of said first counter (CONTUP) upon the arrival of a synchronizing pulse (ZCR) produced by sensing means of the instantaneous position of the motor rotor onto its reset input, a comparator (COMPARATOR) comparing the output of said first register (REG A) with the content of a second resettable counter (CONTSCAN) fed with said master clock signal (ck) and generating a reset pulse of said second counter (CONTSCAN) when the compared information is equal and an incrementing pulse (fscan) for a third counter (CONTN), whose output points one of said stored N samples, **characterized in that** it also comprises

   a programming register (REG FT) storing a certain programmed datum;

   a multiplexer 2*1 (MUX) and a demultiplexer 1*2 (DEMUX) functionally connected to couple the output of said programming register (REG FT) to the input of said first register (REG A) in alternative to the output of said first counter (CONTUP);

   a circuit (MSF FALSE) enabled by a logic command (WAC) generating a forced synchronizing pulse (ZCF) when receiving a (WN) pulse from said third counter (CONTN) when it reaches the value N-1, said forced synchronizing pulse (ZCF) commanding the loading of the datum contained in said programming register (REG FT) in said first register (REG A) during open loop operation, and a resetting signal (CLOSE) of said first counter (CONTUP) and selecting signal of said multiplexer and demultiplexer (MUX, DEMUX).

2. The synchronizing circuit according to claim 1 further comprising a second programming register (REG T) resetting said third counter (CONTN) to a certain value T corresponding to the sample of among said N samples from which said counter starts counting during operation in closed loop mode and the second programmable counter (CONTSCAN) to the programmed value contained in said first programming register (REG FT).

Patentansprüche

1. Schaltung zum Synchronisieren der Phasenumschaltvorgänge eines bürstenlosen Mehrphasenmotors in Übereinstimmung mit einem Profil, das in Form einer Anzahl N digitaler Abtastwerte nichtflüchtig gespeichert ist, die wahlweise zwischen einer Betriebsart mit offener Schleife oder einer Betriebsart mit geschlossener Schleife umgeschaltet werden kann und versehen ist mit einem Frequenzvervielfacher (DIVN) für einen Haupt-Taktsignal (Ck), der ein abgeleitetes Taktsignal (Ck/N) ausgibt, dessen Periode durch einen Faktor N geteilt ist, einem ersten rücksetzbaren Aufwärtszähler (CONTUP), der mit dem abgeleiteten Taktsignal (Ck/N) gespeist wird, einem ersten Register (REG A), das das Ausgangssignal des ersten Zählers (CONTUP) speichert, wenn an dessen Rücksetzeingang ein Synchronisationsimpuls (ZCR), der durch Mittel für die Erfassung der momentanen Position des Motor-Rotors erzeugt wird, ankommt, einem Komparator (COMPARATOR), der das Ausgangssignal des ersten Registers (REG A) mit dem Inhalt eines zweiten rücksetzbaren Zählers (CONTSCAN), der mit dem Haupt-Taktsignal (Ck) gespeist wird, vergleicht und einen Rücksetzimpuls für den zweiten Zähler (CONTSCAN) erzeugt, wenn die verglichenen In-

formationen gleich sind, und einen Inkrementierimpuls (fscan) für einen dritten Zähler (CONTN) erzeugt, dessen Ausgangssignal auf einen der gespeicherten N Abtastwerte zeigt, **dadurch gekennzeichnet, daß** sie außerdem umfaßt:

ein Programmierungsregister (REG FT), das eine bestimmte programmierte Dateneinheit speichert;

einen 2*1-Multiplexer (MUX) und einen 1*2-Demultiplexer (DEMUX), die funktional so angeschlossen sind, daß sie abwechselnd den Ausgang des Programmierungsregisters (REG FT) oder den Ausgang des ersten Zählers (CONTUP) mit dem Eingang des ersten Registers (REG A) koppeln;

eine Schaltung (MSF FALSE), die durch einen Logikbefehl (WAC) freigegeben wird und einen erzwungenen Synchronisationsimpuls (ZCF) erzeugt, wenn sie von dem dritten Zähler (CONTN) einen Impuls (WN) empfängt, wenn dieser den Wert N - 1 erreicht, wobei der erzwungene Synchronisationsimpuls (ZCF) das Laden der in dem Programmierungsregister (REG FT) enthaltenen Dateneinheit in das erste Register (REG A) während des Betriebs mit offener Schleife befiehlt, und einen Rücksetzsignal (CLOSE) für den ersten Zähler (CONTUP) und ein Auswahlsignal für den Multiplexer und den Demultiplexer (MUX, DEMUX) erzeugt.

2. Synchronisationsschaltung nach Anspruch 1, die ferner ein zweites Programmierungsregister (REG T) umfaßt, das den dritten Zähler (CONTN) auf einen bestimmten Wert T zurücksetzt, der demjenigen der N Abtastwerte entspricht, bei dem der Zähler während des Betriebs mit geschlossener Schleife zu zählen beginnt, und den zweiten programmierbaren Zähler (CONTSCAN) auf den programmierten Wert, der in dem ersten Programmierungsregister (REG FT) enthalten ist, zurücksetzt.

Revendications

1. Circuit de synchronisation des commutations de phase d'un moteur polyphasé sans collecteur, selon un profil mémorisé de façon non volatile sous la forme d'un nombre N d'échantillons numériques, commutable sélectivement dans un mode de fonctionnement en boucle ouverte ou en boucle fermée, comprenant un multiplieur de fréquence (DIVN) d'un signal d'horloge maître (CK) générant en sortie un signal d'horloge dérivé (Ck/N) dont la période est divisée par un facteur N, un premier compteur d'incrémentation réinitialisable (CONTUP) piloté par le signal d'horloge dérivé (Ck/N), un premier registre (REG A) mémorisant la sortie du premier compteur (CONTUP) lors de l'apparition d'une impulsion de synchronisation (ZCR) produite par des moyens de détection de la position instantanée du rotor du moteur sur son entrée de réinitialisation, un comparateur (COMPARATOR) comparant la sortie du premier registre (REG A) au contenu d'un second compteur réinitialisable (CONTSCAN) recevant le signal d'horloge maître (ck) et produisant une impulsion de réinitialisation du second compteur (CONTSCAN) quand les informations comparées sont égales et une impulsion d'incrémentation (fscan) pour un troisième compteur (CONTN), dont la sortie indique l'un des N échantillons mémorisés, **caractérisé en ce qu'**il comprend en outre :

un registre de programmation (REG FT) mémorisant une certaine donnée programmée;
un multiplexeur 2*1 (MUX) et un démultiplexeur 1*2 (DEMUX) connectés fonctionnellement de façon à coupler la sortie du registre de programmation (REG FT) à l'entrée, du premier registre (REG A) au lieu de la sortie du premier compteur (CONTUP);
un circuit (MSF FALSE) validé par une commande logique (WAC) générant une impulsion de synchronisation forcée (ZCF) quand il reçoit une impulsion (WN) du troisième compteur (CONTN) quand il atteint la valeur N-1, l'impulsion de synchronisation forcée (ZCF) commandant le chargement de la donnée contenue dans le registre de programmation (REG FT) dans le premier registre (REG A) durant le fonctionnement en boucle ouverte, et un signal (CLOSE) de réinitialisation du premier compteur (CONTUP) et de sélection du signal du multiplexeur et du démultiplexeur (MUX, DEMUX).

2. Circuit de synchronisation selon la revendication 1, comprenant en outre un second registre de programmation (REG T) réinitialisant le troisième compteur (CONTN) à une certaine valeur T correspondant à celui des N échantillons à partir duquel le compteur commence à compter durant le fonctionnement dans le mode en boucle fermée et réinitialisant le second compteur programmable (CONTSCAN) à la valeur programmée contenue dans le premier registre de programmation (REG FT).

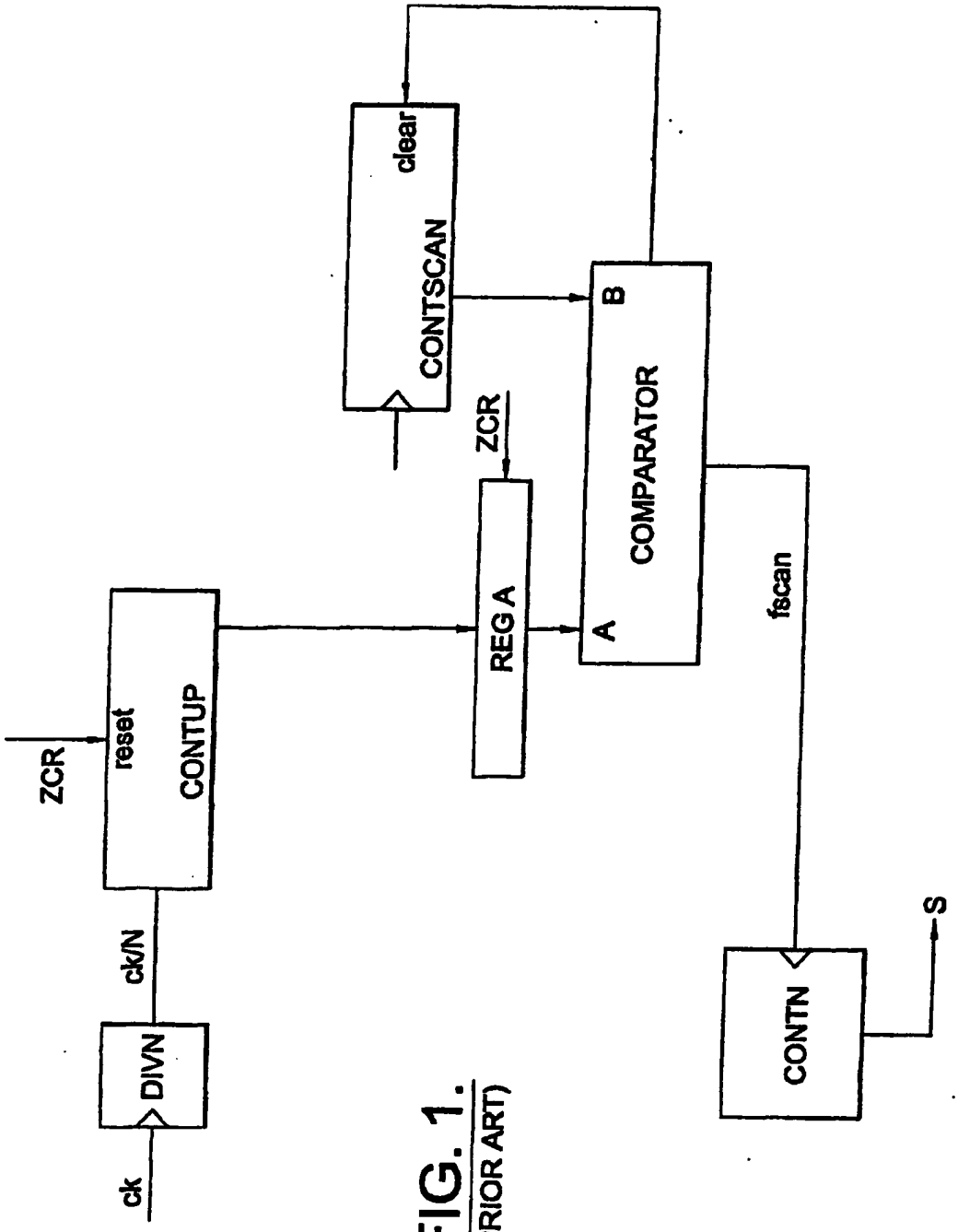

FIG. 1.
(PRIOR ART)

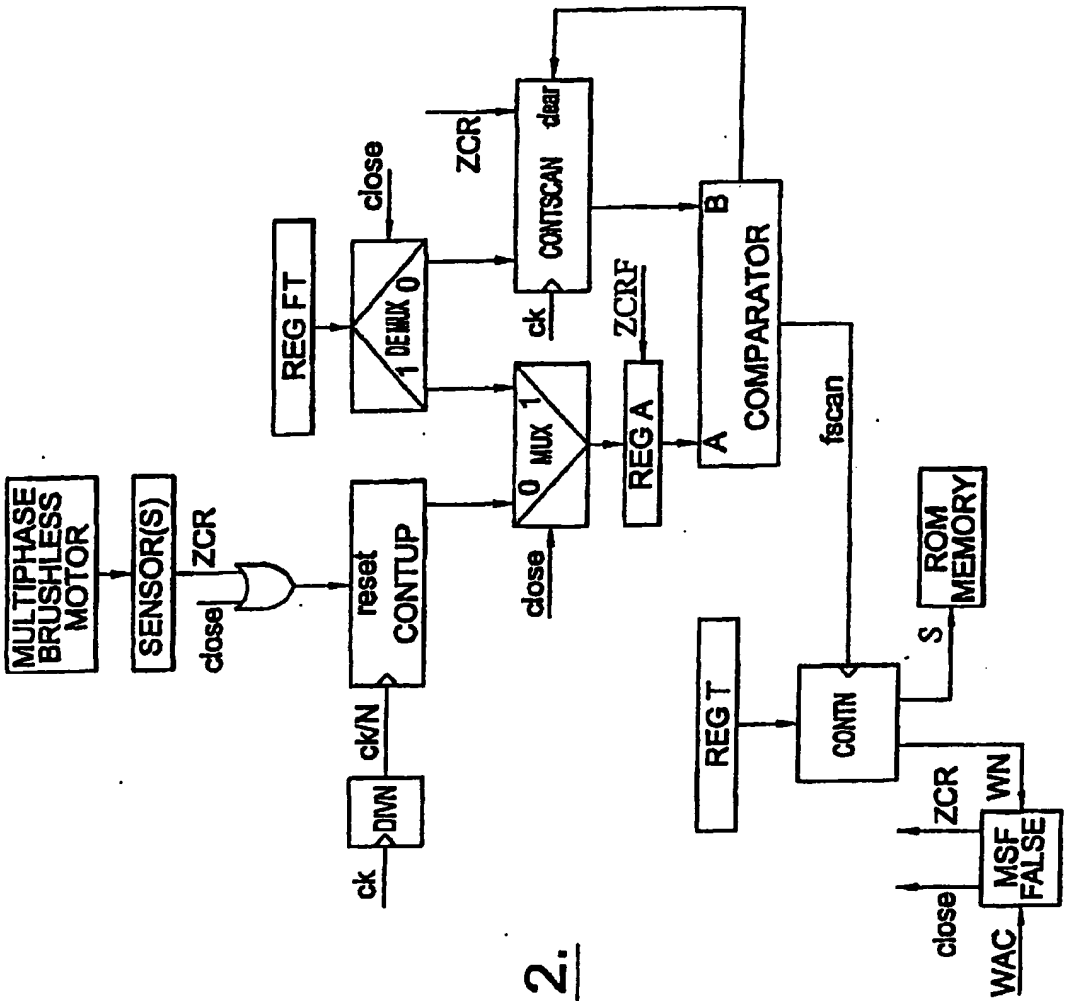
MULTIPHASE BRUSHLESS MOTOR
SENSOR(S)
ZCR
close
reset
CONTUP
ck/N
DIWN
ck
REG FT
close
1 DEMUX 0
ZCR
clear
CONTSCAN
ck
0 MUX 1
close
ZCRF
REG A
A
B
COMPARATOR
fscan
REG T
CONTN
S
ROM MEMORY
ZCR
WN
MSF FALSE
close
WAC

FIG. 2.